



Efficient Performance Trade-off Modeling for Analog Circuit based on Bayesian Neural Network

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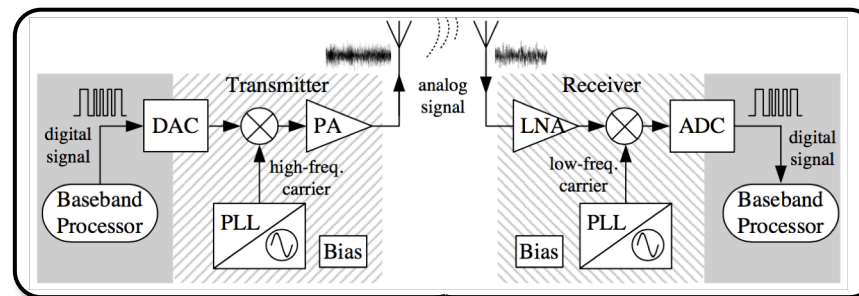
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Hierarchical Optimization for Analog System

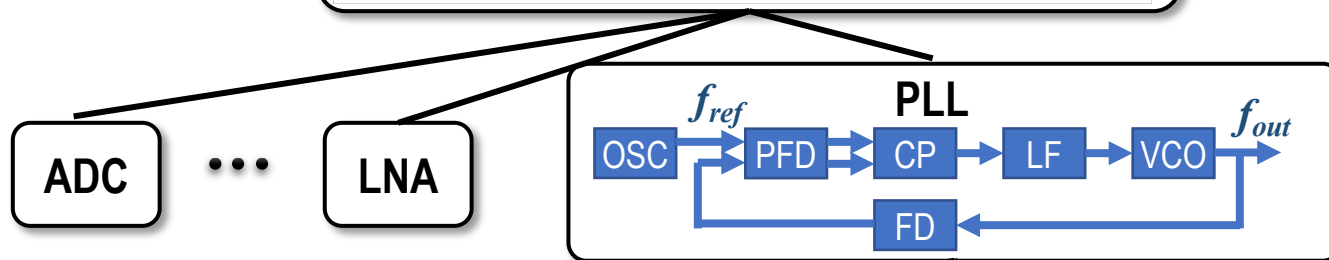
Level 1 (System Level):
e.g., wireless communication system

(constraint mapping)



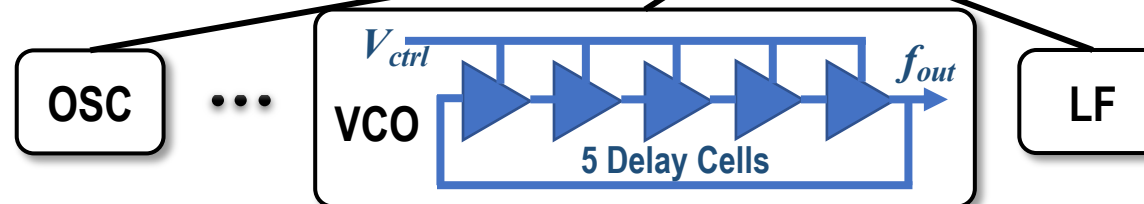
Level 2

(constraint mapping)

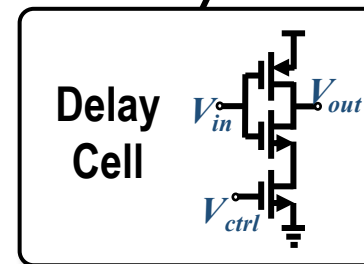


Level 3

(constraint mapping)



Level 4
(Transistor Level)
(transistor sizing)





Hierarchical Optimization for Analog System

Example: PLL Design

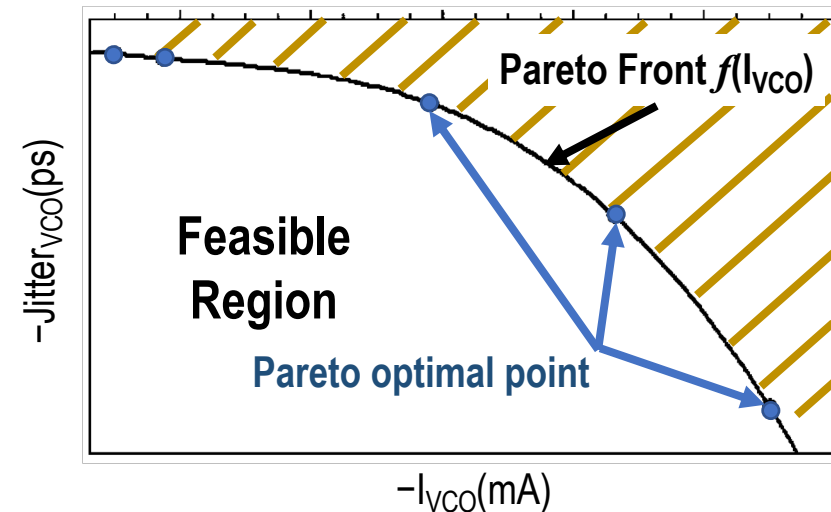
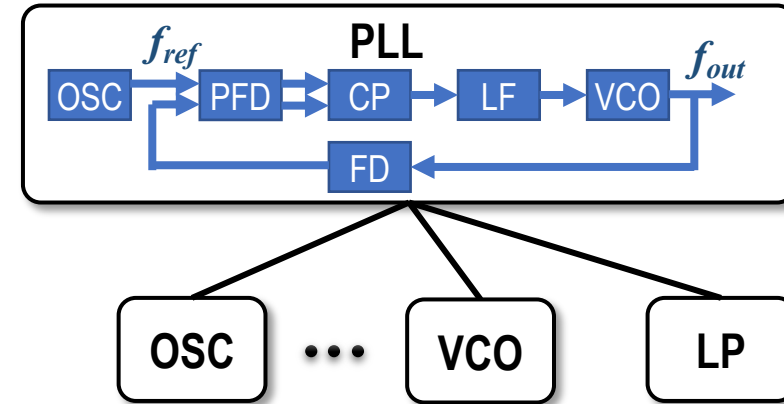
$$\min \text{Power}_{\text{PLL}}(\mathbf{x})$$

$$\text{s.t. PhaseNoise}_{\text{PLL}}(\mathbf{x}) \leq \text{Spec}_{\text{PN}}$$

... ..

Design Parameters \mathbf{x} : I_{LF} , I_{OSC} , I_{VCO} , $\text{Jitter}_{\text{VCO}}$, ...

Behavioral Models : $\text{Power}_{\text{PLL}}(\mathbf{x})$, $\text{PhaseNoise}_{\text{PLL}}(\mathbf{x})$





Hierarchical Optimization for Analog System

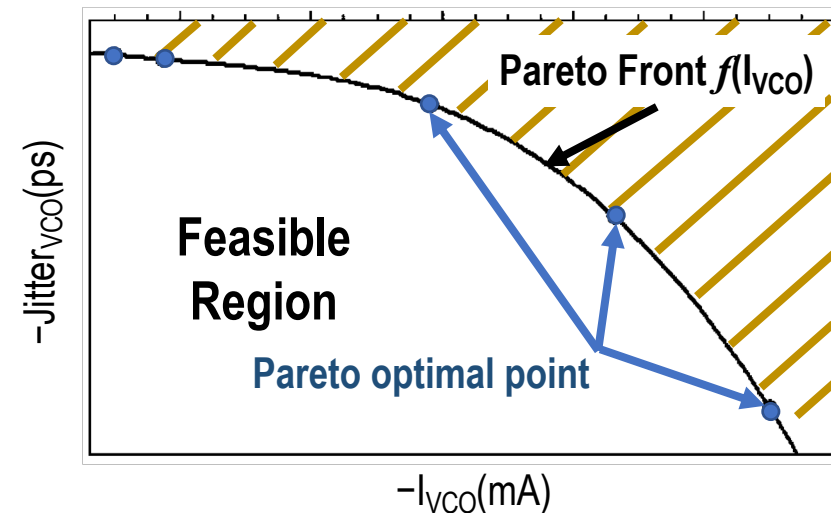
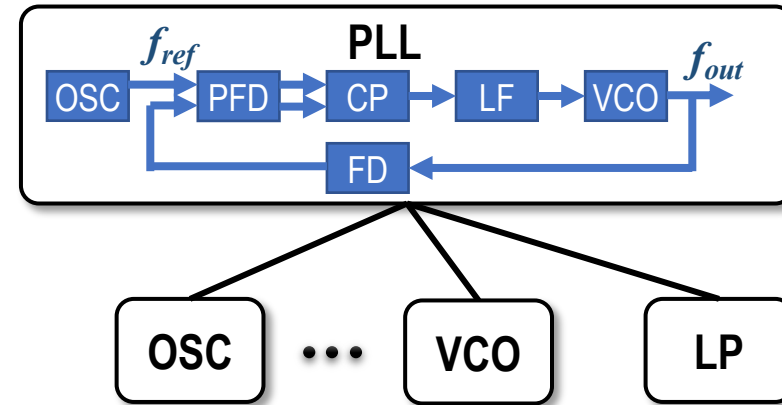
Example: PLL Design

$$\begin{aligned} & \min \text{Power}_{\text{PLL}}(\mathbf{x}) \\ & \text{s.t. } \text{PhaseNoise}_{\text{PLL}}(\mathbf{x}) \leq \text{Spec}_{\text{PN}} \\ & \quad -\text{Jitter}_{\text{VCO}} \leq f(I_{\text{VCO}}) \\ & \quad \dots \dots \end{aligned}$$

Design Parameters \mathbf{x} : I_{LP} , I_{OSC} , I_{VCO} , $\text{Jitter}_{\text{VCO}}$, ...

Behavioral Models : $\text{Power}_{\text{PLL}}(\mathbf{x})$, $\text{PhaseNoise}_{\text{PLL}}(\mathbf{x})$

Pareto Front (PF) : $f(I_{\text{VCO}})$





Pareto Front (PF) Modeling

- **Goal: Obtain trade-off models among different Pols**
- **Many methods exist in the literature --- solve multi-objective optimization**
 - Simulation-based
 - Normal Boundary Intersection
 - Successive Pareto Optimization
 - WATSON, MOEA/D, NSGA-II
 - GP model-based
 - GPMOOG, MOBO
 - Square exponential covariance function:

$$k(\mathbf{x}_i, \mathbf{x}_j) = \theta_1 \cdot \exp\left(-\theta_2 \cdot \|\mathbf{x}_i - \mathbf{x}_j\|^2\right)$$

$\mathbf{x}_i, \mathbf{x}_j$: design variables

θ_1, θ_2 : Hyper-parameters

- **Obtain PF model based on Bayesian Neural Network with few sims**



Pareto Front Modeling

- Problem definition

- $\mathbf{f} = \mathbf{f}(\mathbf{x})$ dominant $\mathbf{f}^* = \mathbf{f}(\mathbf{x}^*)$

$$\mathbf{f} \neq \mathbf{f}^* \text{ and } f_i \leq f_i^* \quad i = 1, 2, \dots, m$$

$\mathbf{x} \in \Omega \subseteq \mathcal{R}^d$: design variables

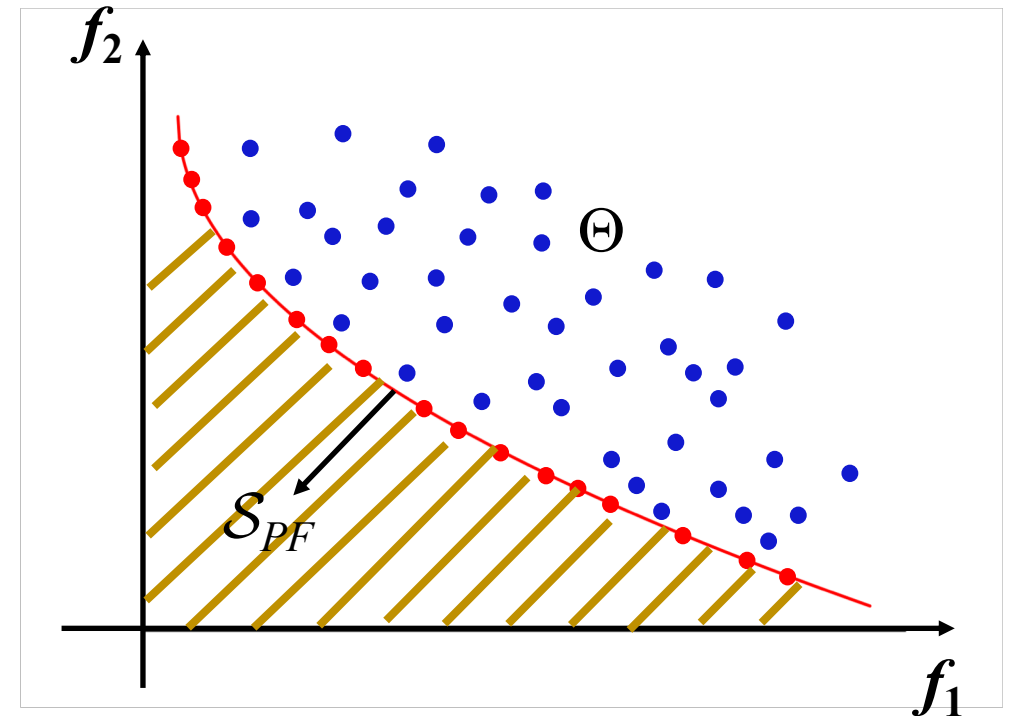
$\mathbf{f}(\mathbf{x}) \in \Theta \subseteq \mathcal{R}^m$: Pols of analog circuit

- No \mathbf{f} in Θ dominant \mathbf{f}^* , \mathbf{f}^* is Pareto optimal point, \mathbf{x}^* is Pareto optimal design
- \mathcal{S}_{PS} and \mathcal{S}_{PF} can be obtained by

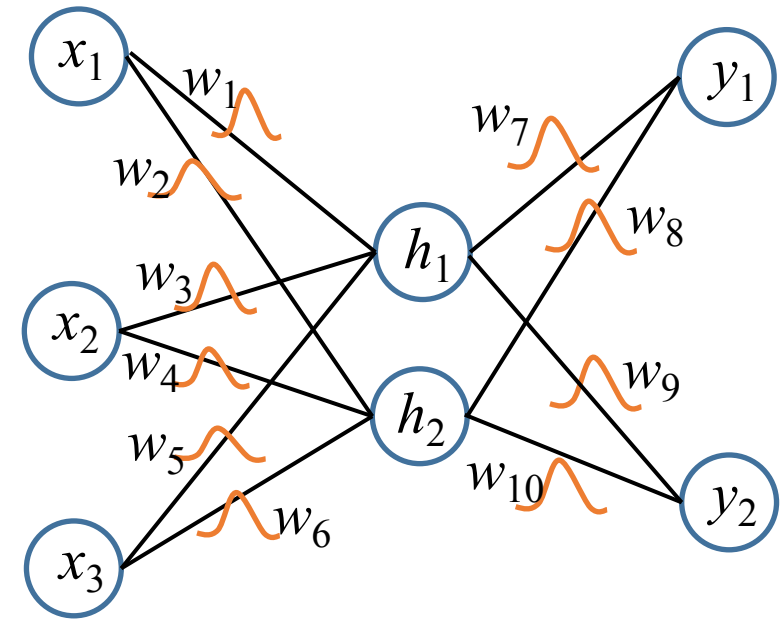
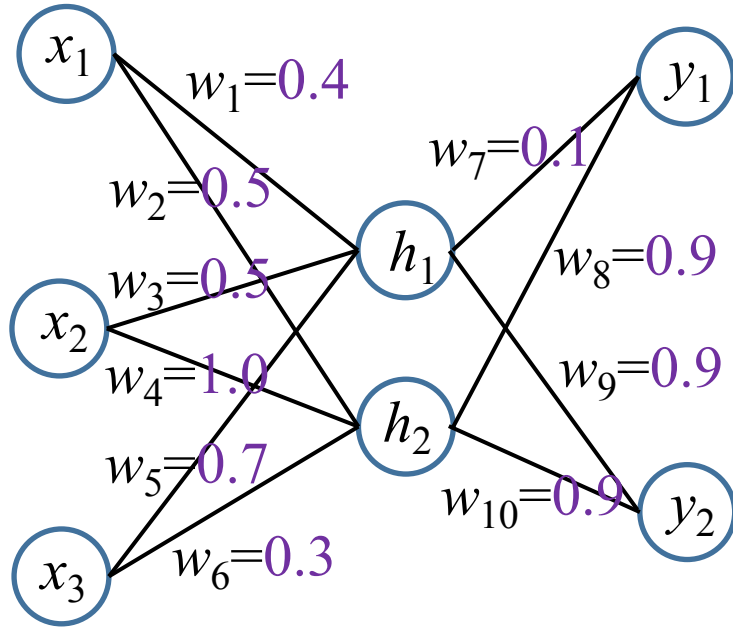
$$\min_{\mathbf{x} \in \Omega} \mathbf{f}(\mathbf{x}) = [f_1(\mathbf{x}) \quad f_2(\mathbf{x}) \quad \dots \quad f_m(\mathbf{x})]^T$$

\mathcal{S}_{PS} : all Pareto optimal design

\mathcal{S}_{PF} : all Pareto optimal point



Bayesian Neural Network



- **Conventional neural network**
 - Parameters are deterministic
 - Deterministic prediction

- **Bayesian neural network (BNN)**
 - Parameters satisfy PDFs
 - Probabilistic prediction



Bayesian Neural Network

• **Prior** $p(\mathbf{w}|\alpha) = N(\mathbf{w}|0, \alpha^{-1}\mathbf{I})$

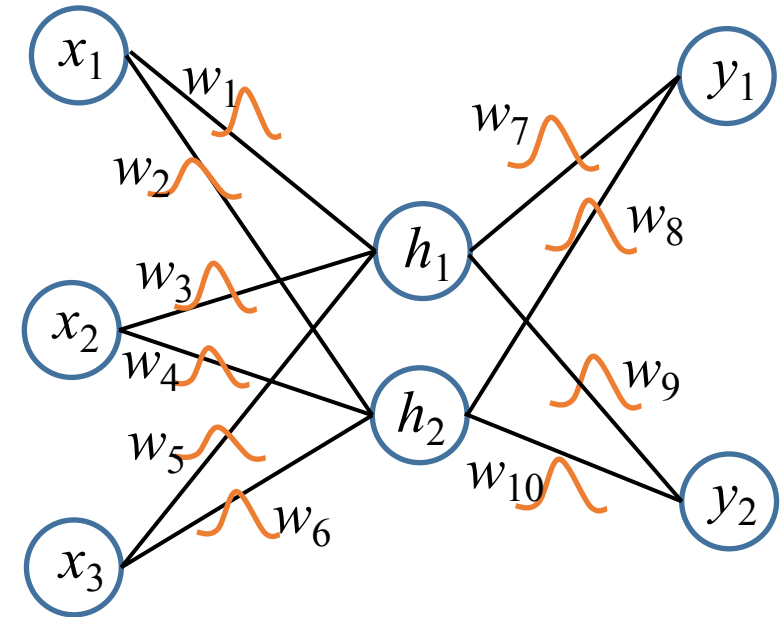
• **Likelihood**

$$\mathbf{f}(\mathbf{x}) = \mathbf{y}(\mathbf{x}, \mathbf{w}) + \boldsymbol{\varepsilon}, \text{ where } \boldsymbol{\varepsilon} \sim N(\boldsymbol{\varepsilon}|\mathbf{0}, \beta^{-1}\mathbf{I})$$

$$\Rightarrow p(\mathbf{f}|\mathbf{x}, \mathbf{w}, \beta) = N(\mathbf{f}|\mathbf{y}(\mathbf{x}, \mathbf{w}), \beta^{-1}\mathbf{I})$$

$$\mathcal{D} = \{(\mathbf{x}_i, \mathbf{f}_i) | i = 1, 2, \dots, N\}$$

$$p(\mathcal{D}|\mathbf{w}, \beta) = \prod_{i=1}^N p(\mathbf{f}_i|\mathbf{x}_i, \mathbf{w}, \beta) \\ = \prod_{i=1}^N N(\mathbf{f}_i|\mathbf{y}(\mathbf{x}_i, \mathbf{w}), \beta^{-1}\mathbf{I})$$



$\mathbf{w} = [w_1 \ w_2 \ \dots \ w_W]^T$:

$\mathbf{y}(\mathbf{x}, \mathbf{w}) \subseteq \mathcal{R}^m$:

$\boldsymbol{\varepsilon} \subseteq \mathcal{R}^m$:

\mathcal{D} :

α, β :

BNN weights

BNN Ppls prediction

approximation error

training data set

precision(inverse of variance)



Bayesian Neural Network

- **Prior** $p(\mathbf{w}|\alpha) = N(\mathbf{w}|0, \alpha^{-1}\mathbf{I})$

- **Likelihood**

$$p(\mathcal{D}|\mathbf{w}, \beta) = \prod_{i=1}^N N(\mathbf{f}_i | \mathbf{y}(\mathbf{x}_i, \mathbf{w}), \beta^{-1}\mathbf{I})$$

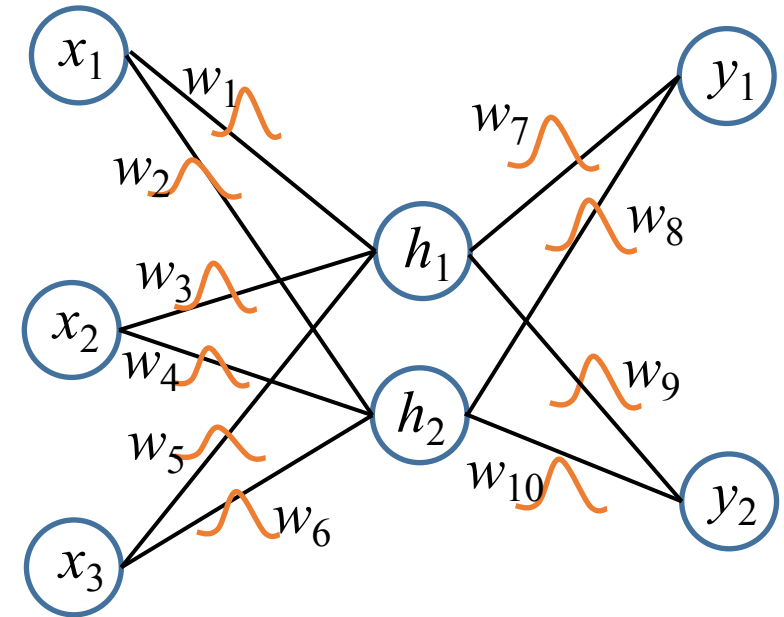
- **Posterior**

Bayes Theorem: Posterior \propto Prior \times Likelihood, i.e.,

$$p(\mathbf{w}|\mathcal{D}, \alpha, \beta) \propto p(\mathbf{w}|\alpha) \cdot p(\mathcal{D}|\mathbf{w}, \beta)$$

- **Predictive function**

$$\begin{aligned} p(\mathbf{f}|\mathbf{x}, \mathcal{D}, \alpha, \beta) &= \int p(\mathbf{f}|\mathbf{x}, \mathbf{w}, \beta) \cdot p(\mathbf{w}|\mathcal{D}, \alpha, \beta) d\mathbf{w} \\ &= \int N(\mathbf{f}|\mathbf{y}(\mathbf{x}, \mathbf{w}), \beta^{-1}\mathbf{I}) \cdot p(\mathbf{w}|\mathcal{D}, \alpha, \beta) d\mathbf{w} \end{aligned}$$





Bayesian Neural Network

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- **Likelihood**

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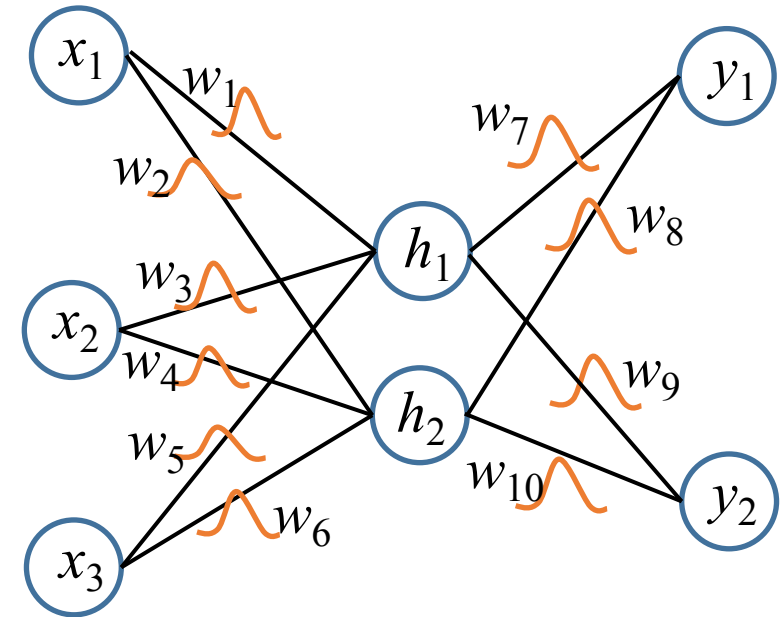
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Bayesian Neural Network

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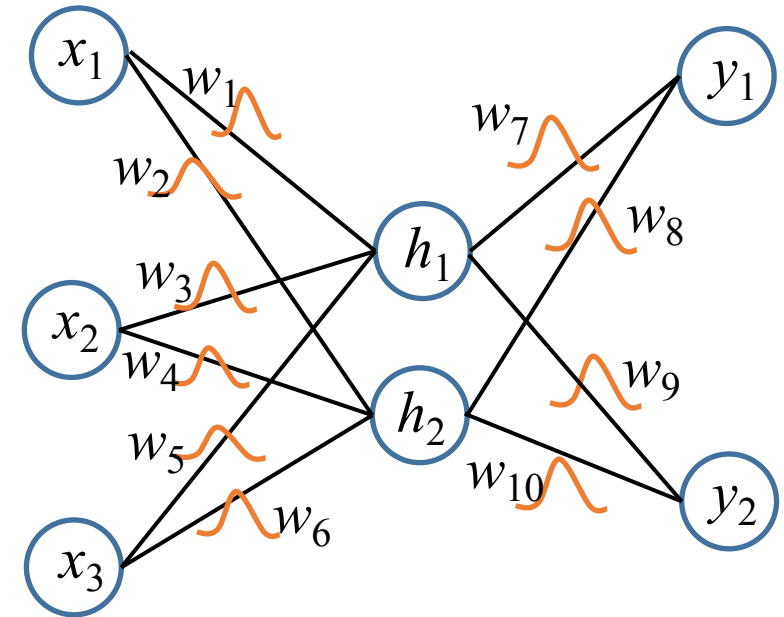
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Bayesian Neural Network

- **Approximate Posterior**

$$\max_{\phi} L(\phi) = \mathbb{E}_{q(\mathbf{w}|\phi)} [\log p(\mathbf{w}, \mathcal{D}, \alpha, \beta) - \log q(\mathbf{w}|\phi)]$$

$$s.t. \quad \text{supp}[q(\mathbf{w}|\phi)] \subseteq \text{supp}[p(\mathbf{w}|\mathcal{D}, \alpha, \beta)]$$

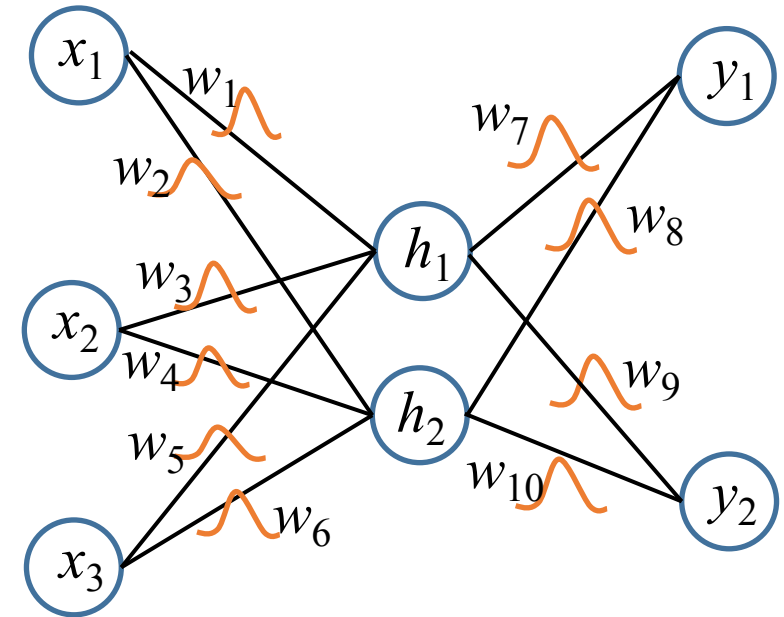
- Automatic differential variational inference (ADVI)

$$\Rightarrow q(\mathbf{w}|\phi^*)$$

- **Predictive function**

$$p(\mathbf{f}|\mathbf{x}, \mathcal{D}, \alpha, \beta) = \int p(\mathbf{f}|\mathbf{x}, \mathbf{w}, \beta) \cdot p(\mathbf{w}|\mathcal{D}, \alpha, \beta) d\mathbf{w}$$

$$\approx \int N(\mathbf{f}|\mathbf{y}(\mathbf{x}, \mathbf{w}), \beta^{-1}\mathbf{I}) \cdot q(\mathbf{w}|\phi^*) d\mathbf{w}$$



$q(\mathbf{w}|\phi)$:

$\text{supp}[q(\mathbf{w}|\phi)]$:

$\text{supp}[p(\mathbf{w}|\mathcal{D}, \alpha, \beta)]$:

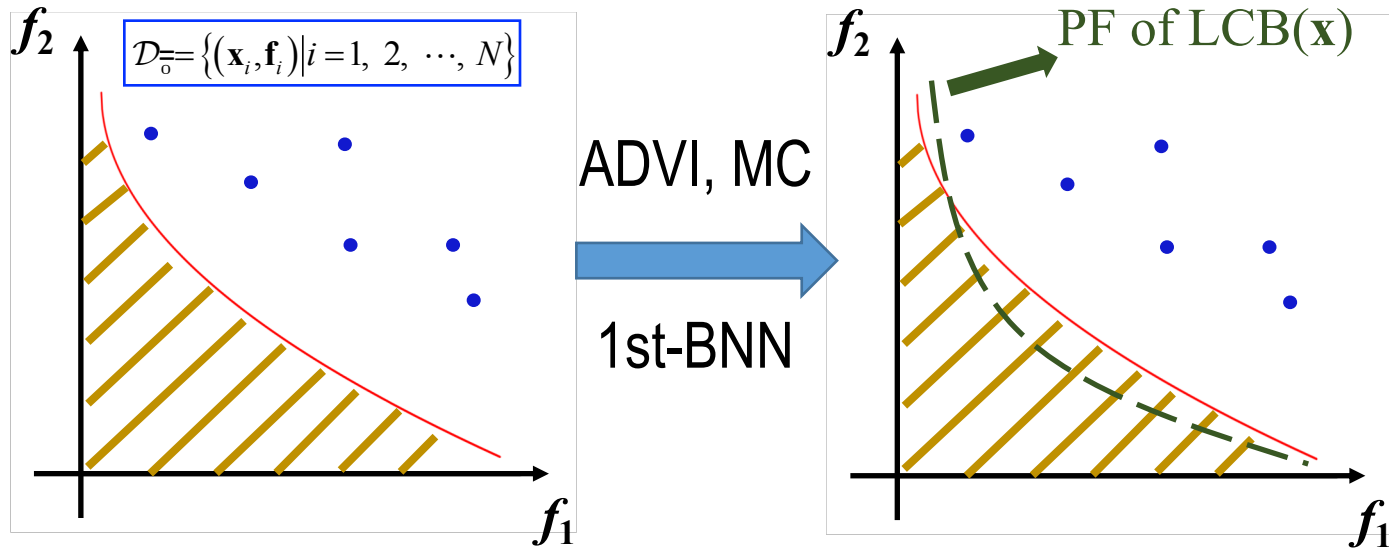
PDF parametrized by ϕ

domain of $q(\mathbf{w}|\phi)$

domain of $p(\mathbf{w}|\mathcal{D}, \alpha, \beta)$



Pareto Front Modeling based on BNN

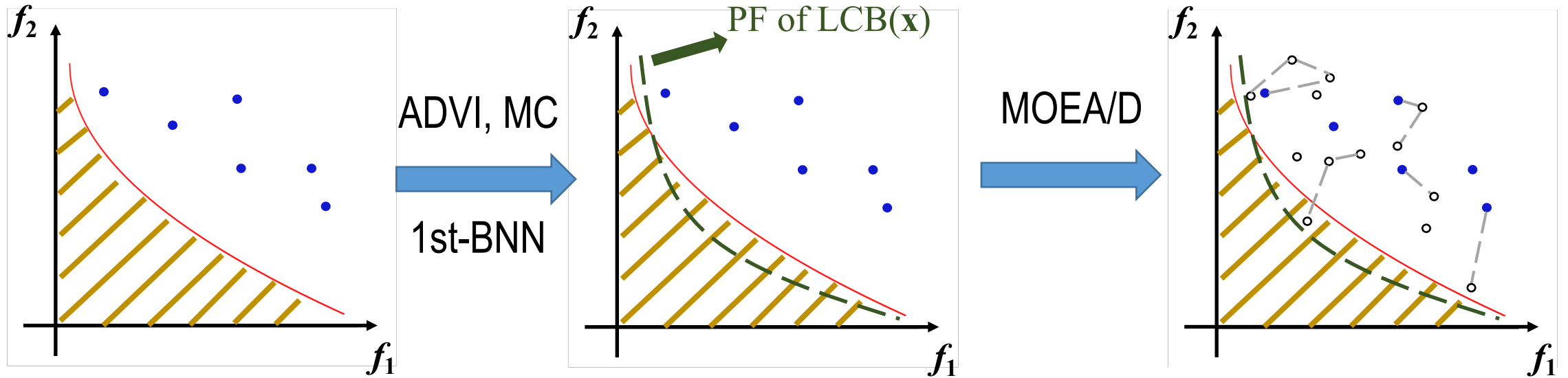


$$\text{LCB}(\mathbf{x}) = \text{mean}[\mathbf{f}(\mathbf{x})] - K \cdot \text{var}[\mathbf{f}(\mathbf{x})]$$

K : balance sampling process



Pareto Front Modeling based on BNN



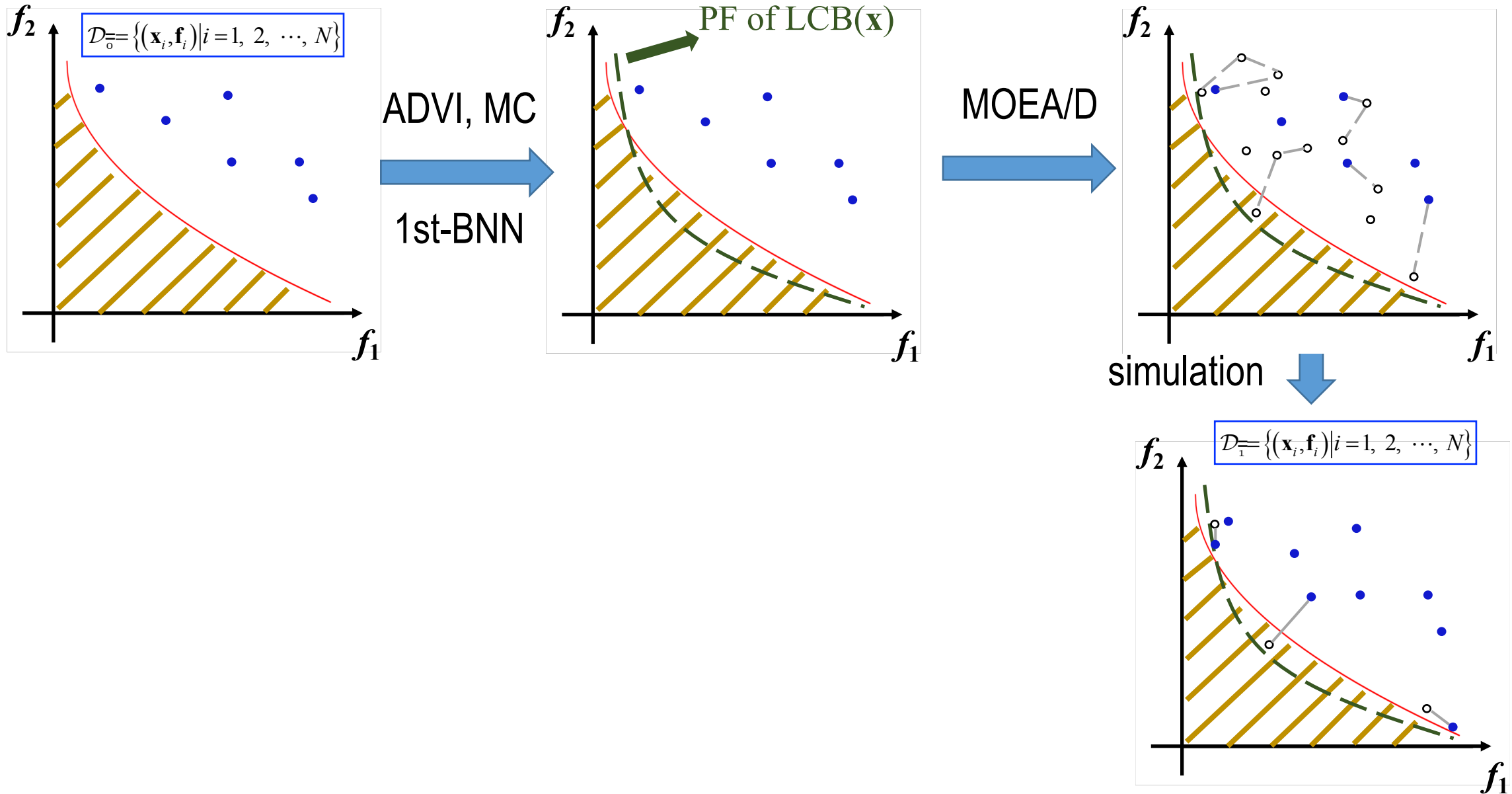
$$\text{LCB}(\mathbf{x}) = \text{mean}[\mathbf{f}(\mathbf{x})] - K \cdot \text{var}[\mathbf{f}(\mathbf{x})]$$

K : balance sampling process

ρ : sampling ratio, $\#black / (\#black + \#blue)$

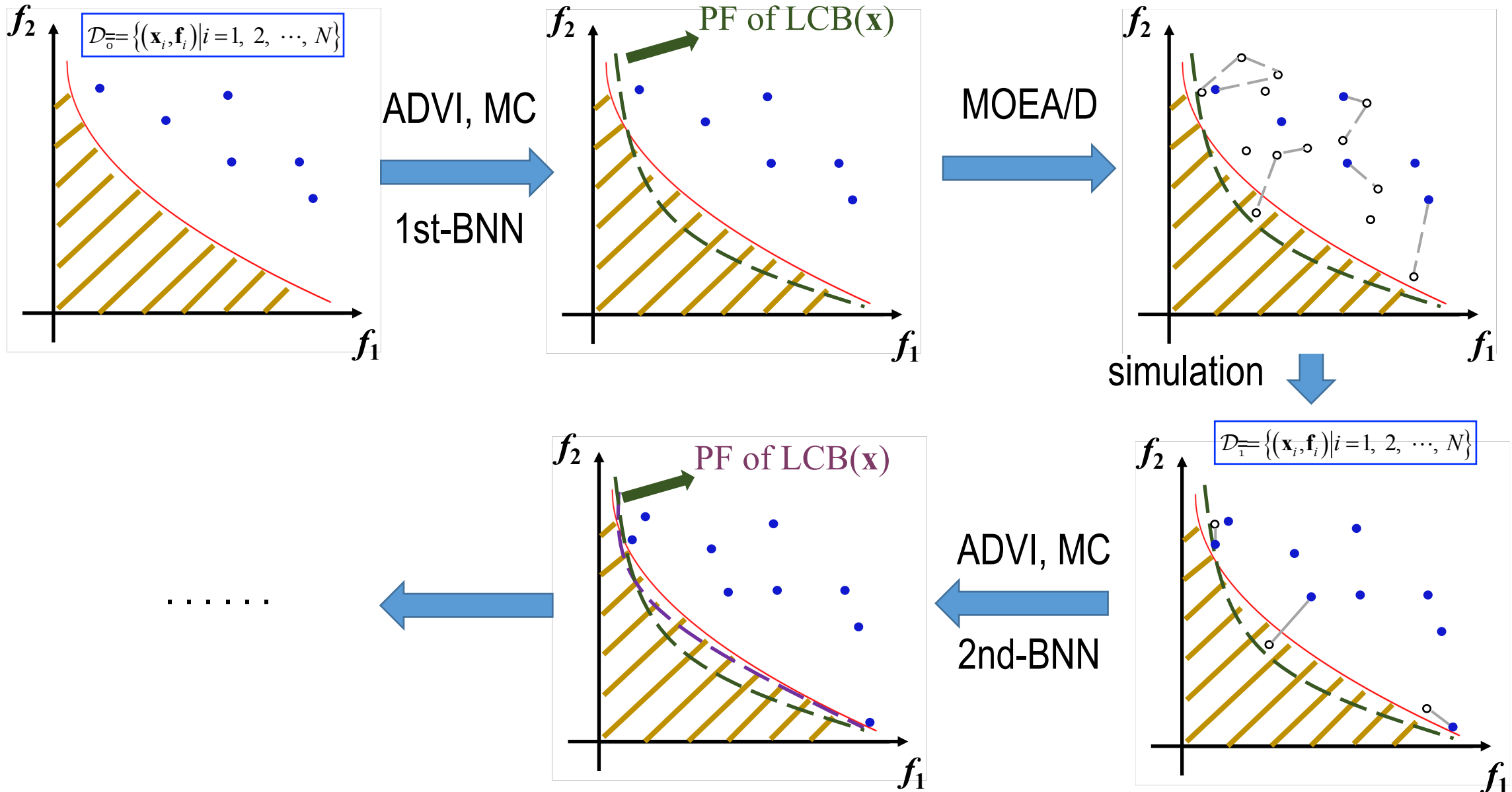


Pareto Front Modeling based on BNN





Pareto Front Modeling based on BNN



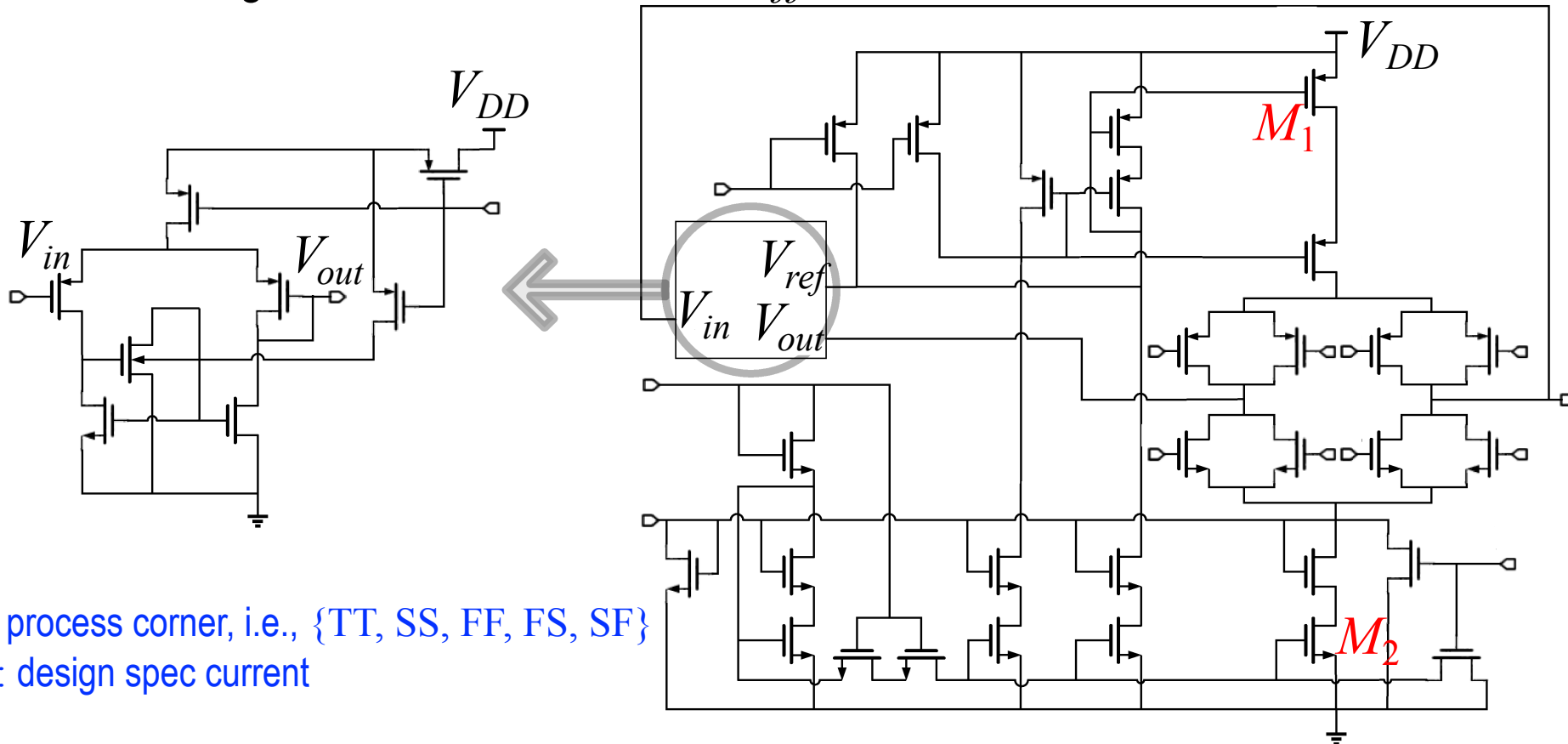
Example1: Charge Pump

- 40nm CMOS Technology
- Performance metrics: (*devi*, *diff*)
- 16 design variables
- Good design: small *devi* and small *diff*

$$diff = \max_{\Lambda} (I_{M_1,max} - I_{M_1,avg}) + \max_{\Lambda} (I_{M_1,avg} - I_{M_1,min})$$

$$+ \max_{\Lambda} (I_{M_2,max} - I_{M_2,avg}) + \max_{\Lambda} (I_{M_2,avg} - I_{M_2,min})$$

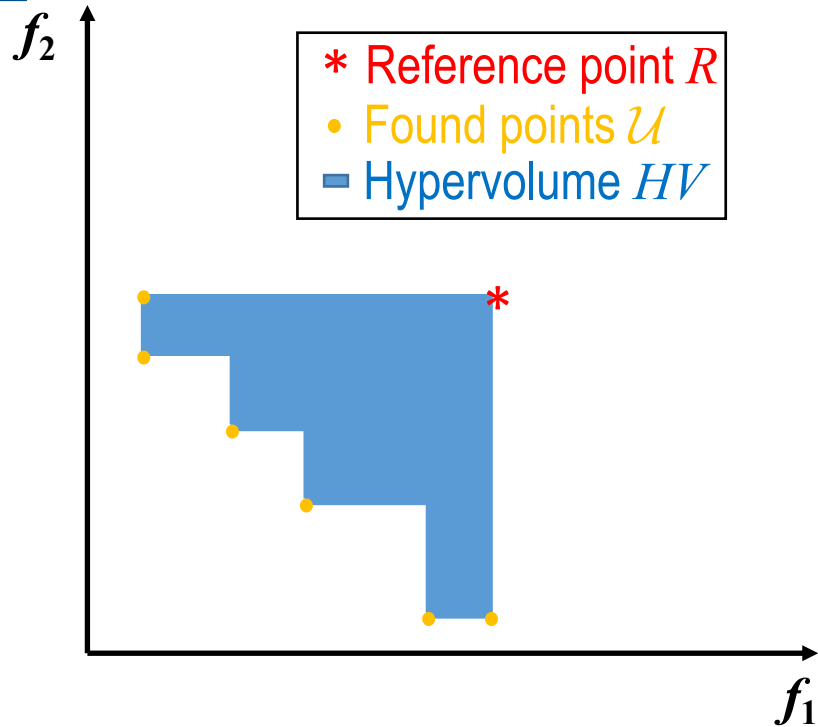
$$devi = \max_{\Lambda} |I_{M_1,avg} - I_{sta}| + \max_{\Lambda} |I_{M_2,avg} - I_{sta}|$$



Λ : process corner, i.e., {TT, SS, FF, FS, SF}
 I_{sta} : design spec current



Example1: Charge Pump



- HV measures the quality of PF
- HV maximizes when \mathcal{U} is exact PF

- Limit the number of allowed transistor-level simulations
- BNN: two hidden layers with 25 and 10 hidden units.
- BNNBO achieves small “Min *devi*”, “Min *diff*” and large HV

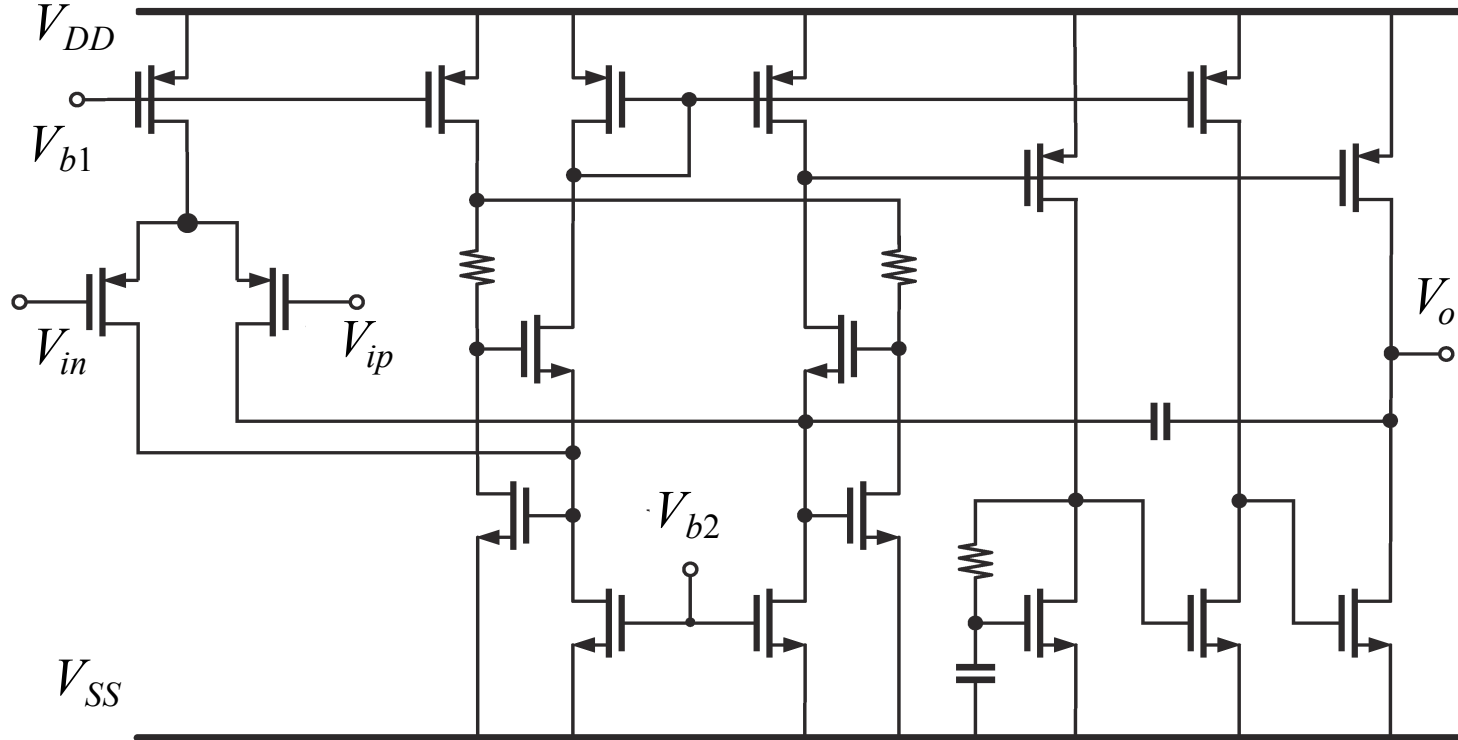
| Method | HV | Min <i>devi</i> | Min <i>diff</i> |
|------------------|-----------------|-----------------|-----------------|
| BNNBO-150 | 15046.55 | 0.19 | 137.32 |
| MOEA/D-150 | 14076.10 | 0.33 | 179.58 |
| MOBO-150 | 14263.70 | 0.27 | 174.84 |
| MOEA/D-300 | 14248.47 | 0.33 | 174.56 |
| MOBO-300 | 14285.07 | 0.26 | 174.35 |



Example2: Low-Power Amplifier

- 40nm CMOS Technology
- Performance metrics $Gain_w = \min_{\Lambda} Gain$, $UGF_w = \min_{\Lambda} UGF$, $PM_w = \min_{\Lambda} PM$
- 13 design variables

Λ : process corner, i.e., {TT, SS, FF, FS, SF}





Example2: Low-Power Amplifier

| Method | HV | Max $Gain_w$ | Max UGF_w | Max PM_w |
|------------------|-----------------|---------------|-------------|--------------|
| BNNBO-200 | 10725.00 | 101.78 | 1.23 | 93.74 |
| MOEA/D-200 | 6036.89 | 68.87 | 0.98 | 72.96 |
| MOBO-200 | 8001.19 | 84.78 | 1.20 | 74.39 |
| MOEA/D-400 | 9456.72 | 103.77 | 1.16 | 74.46 |
| MOBO-400 | 9938.76 | 99.84 | 1.22 | 77.18 |

- The discrepancy in Max $Gain_w$ is small enough to be neglected
- BNNBO-200 performs better than MOEA/D-400 and MOBO-400.



Conclusions

- **Bayesian Neural Network (BNN)**
 - Trained by ADVI method
 - Probabilistic prediction obtained by MC method
- **Bayesian Optimization**
 - Solve the optimum of LCB function by modified MOEA/D
 - LCB asymptotically approaches true PF
- **Future work**
 - BNN structure for different circuits

